

FIG. 1A is a schematic diagram of a transistor circuit. FIG. 1B is a graph of Log Drain Current (I_D) versus Gate Voltage (V_{gate}) for the circuit of FIG. 1A.

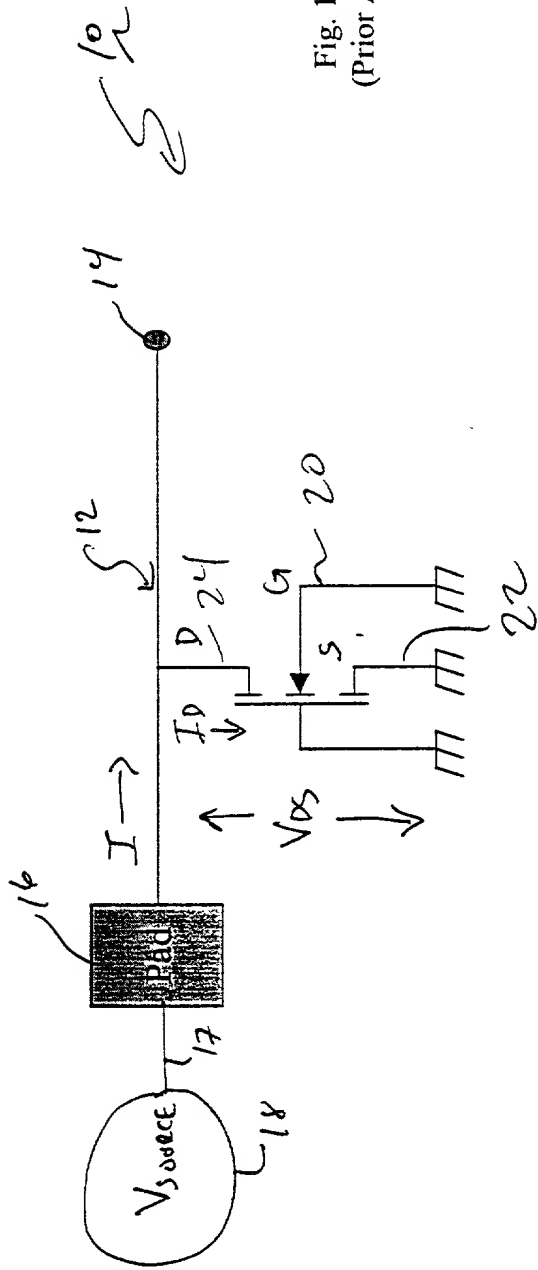


Fig. 1A
(Prior Art)

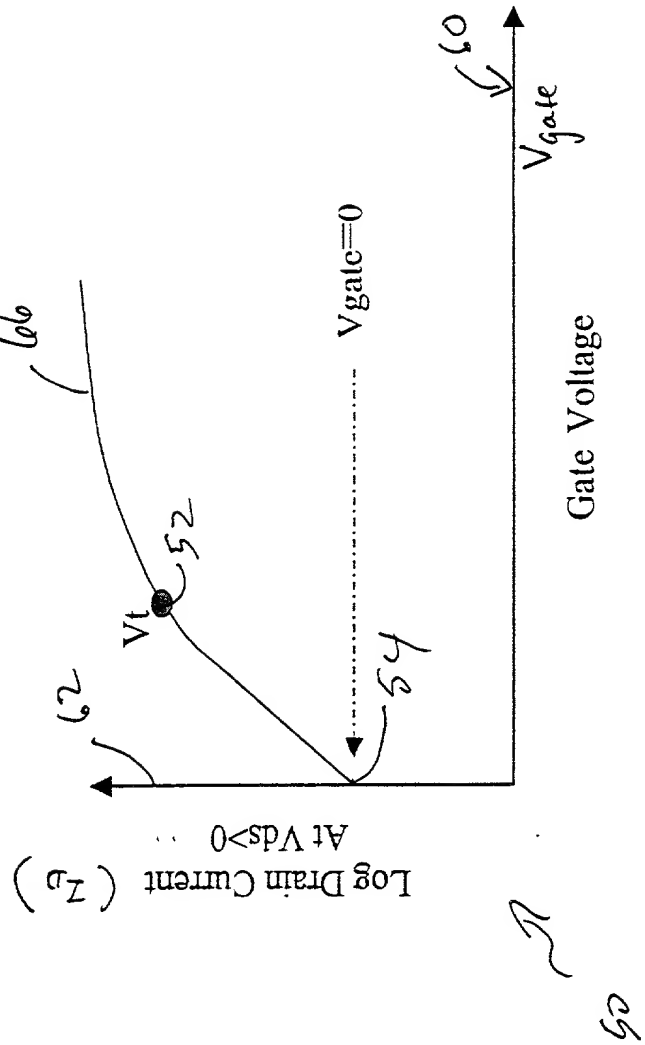


Fig. 1B
(Prior Art)

FIG. 1C

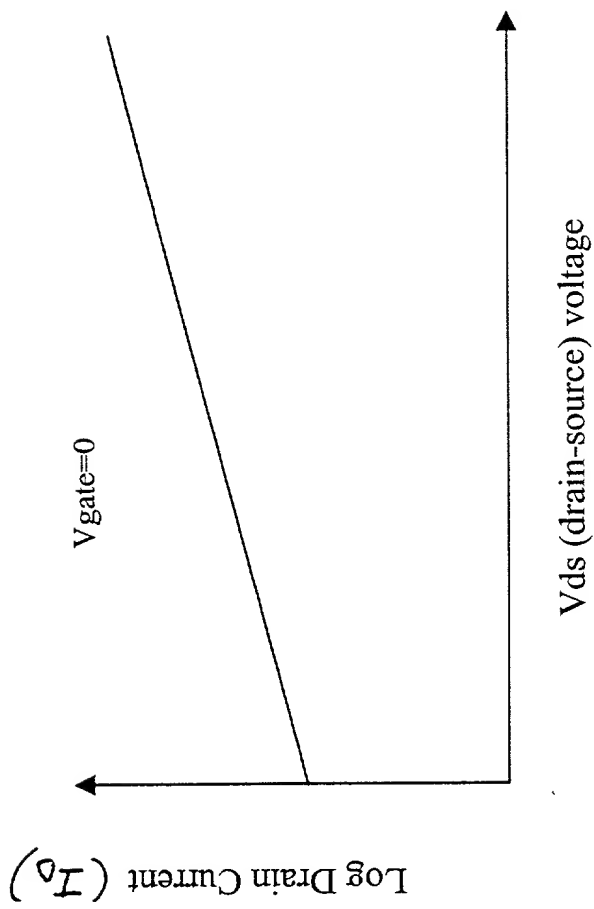


Fig. 1C
(Prior Art)

Fig. 2A

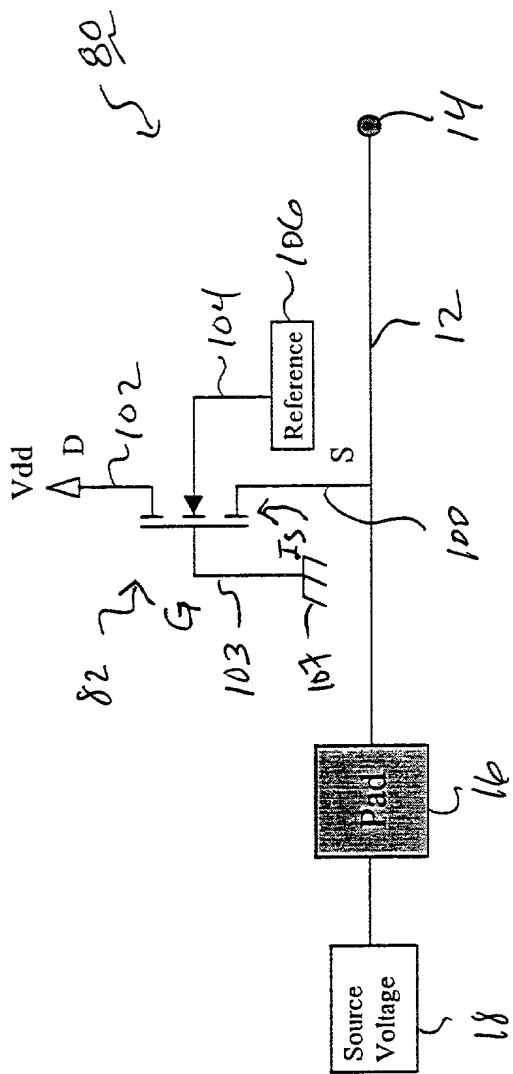
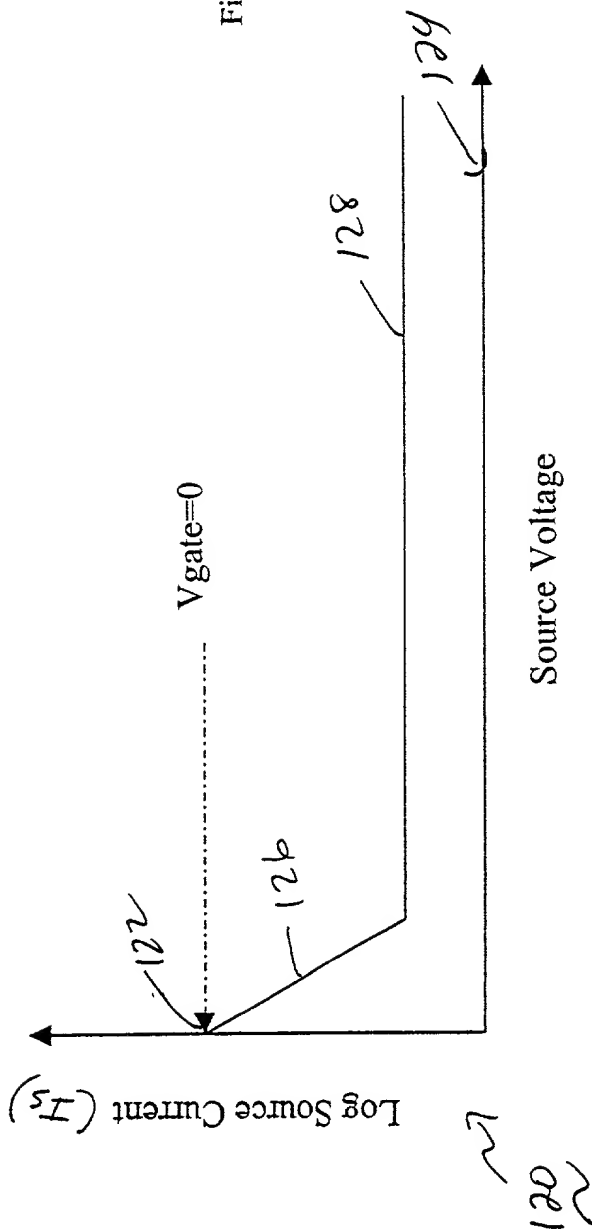


Fig. 2B



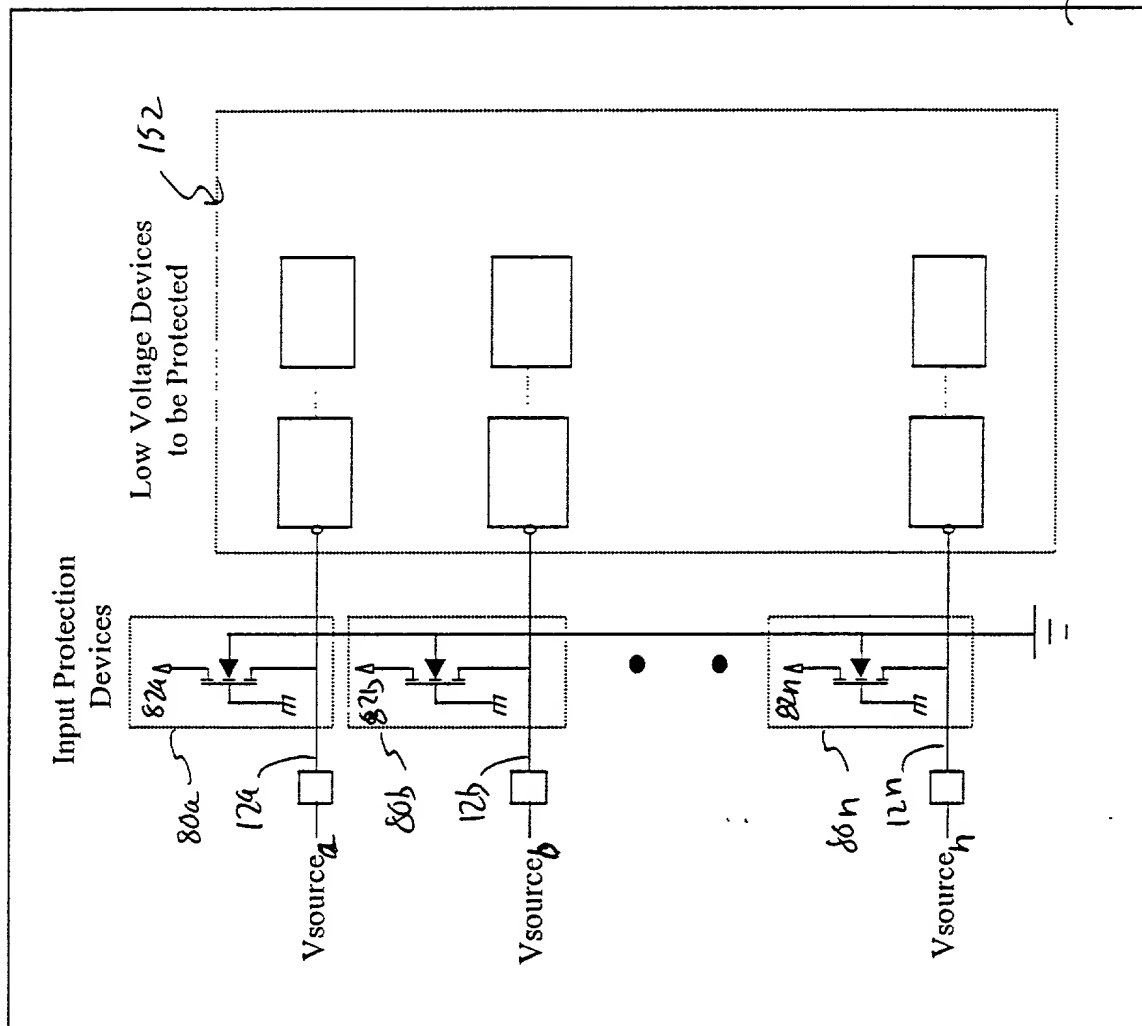


Fig. 3